

## **CXL™ Consortium Members – Statements of Support for CXL 3.0 Specification**

### **AMD**

“CXL has always been about opening up possibilities for dynamic and flexible infrastructure. CXL is fundamental to accelerating modern workload types, each with their own coherency, latency, and pooling requirements. CXL 3.0 brings us closer to truly effective heterogeneous computing that maximizes performance and allows us to deliver the value of flexible compute to our customers in enterprise, cloud and edge.”

*Robert Hormuth, corporate vice president, Data Center Solutions Group, AMD*

### **Arm**

“Standardization remains critical to delivering the compute required for increasingly complex datacenter workloads. Arm’s collaboration with consortium members on the CXL 3.0 specification will enable more performance and flexibility, allowing customers to build and deploy scalable, heterogeneous systems that best match their needs.”

*Andy Rose, chief system architect and fellow, Architecture and Technology Group, Arm*

### **Astera Labs**

“The new CXL 3.0 Specification doubles bandwidth, enhances fabric management, and expands the scale of heterogenous compute, resulting in significant optimizations for AI and Machine Learning. Astera Labs is proud to collaborate with the CXL Consortium in the development of the new specification and we look forward to leveraging CXL 3.0 to expand our portfolio of purpose-built connectivity solutions.”

*Jitendra Mohan, CEO, Astera Labs*

### **Cadence**

“The CXL Consortium has introduced the CXL 3.0 specification to meet the needs of increasingly compute-intensive AI and ML applications. Cadence has been an active member of the CXL Consortium, demonstrating the industry’s first complete CXL IP solution in silicon. Cadence IP implements the CXL 3.0 features enabling 64GT/s transfers at low latency with the latest IDE specification for security while maintaining backward compatibility. This enables customers to build robust, high-performance solutions while lowering risk and reducing development cost.”

*Rishi Chugh, vice president, product marketing and management, IP Group, Cadence*

### **Elastics.cloud**

“At Elastics.cloud we’ve been pleased to be part of the CXL specification journey, helping to create a broad and open ecosystem alongside the consortium’s 200+ members. As our customers are developing next-generation architectures, we see that cloud, edge, and enterprise solutions require resource pooling and composability to manage increasing volumes of data effectively and affordably. We look forward to the upcoming additions to the CXL 3.0 specification – increased bandwidth, multi-level switching, and fabric-based designs – which will add significant functionality to the interconnect for even more robust solutions.”

*George Apostol, CEO, Elastics.cloud*

### **Google Cloud**

“As traditional Moore’s law improvements slow, Google Cloud is using custom accelerators, such as Tensor Processing Units (TPUs) and Video Coding Units (VCUs) to continue to sustainably scale performance. We are excited by the CXL 3.0 enhancements, such as fabric capabilities and peer-to-peer

communication, that will enable such accelerators to be used more efficiently and bring more value to our customers.”

*Amber Huffman, principal engineer, Google Cloud*

#### **HPE**

“To support growing demands in the performance and scale of HPC and AI applications that are becoming more complex and data-intensive, future data center technologies will involve disaggregated, heterogeneous, memory-centric computing capabilities. Embracing a standard protocol to support memory and fabric solutions across these architectures will become a key requirement. The release of the CXL 3.0 specification is an important milestone as it delivers new levels of switching and fabric capabilities, in a standardized way, helping to ease design and deployment of next-generation technologies.”

*Michael Woodacre, HPE Fellow and VP, CTO, HPC and AI, HPE*

#### **Intel**

“Intel is excited to see the CXL Consortium launching the CXL 3.0 Specification, which will open many new innovative usages around disaggregated compute architectures with pooled and shared resources such as memory and accelerators at the Rack level and beyond. CXL has become the focal point for the advancement of high-speed IO with coherency and memory enhancements and Intel remains committed to working with the industry to continue to drive the CXL technology through the CXL Consortium.”

*Dr. Debendra Das Sharma, senior fellow, and co-GM of Memory and I/O Technologies, Intel Corporation and CXL Consortium Technical Task Force Co-Chair*

#### **Lenovo Infrastructure Solutions Group**

“As an active member of the CXL Consortium, Lenovo is committed to developing this important standard and helping build the ecosystem around the new CXL interconnect. We are excited to be part of developing solutions that enable a new era of data center performance and efficiency, working with the consortium to identify specifications that foster the growth and adoption of innovative CXL products.”

*Greg Huff, chief technology officer, Lenovo Infrastructure Solutions Group*

#### **Liquid**

“Liquid is excited to collaborate with the other talented CXL Consortium members to achieve infrastructure holy grail status with the CXL 3.0 specification, finally disaggregating DRAM from CPU for unprecedented memory utilization. This emerging CXL-based ecosystem enables Liquid customers to disaggregate and compose memory in tandem with accelerators and CPU for new levels resource efficiency and performance while significantly reducing power and cooling requirements associated with modern, AI-driven computing.”

*Ben Bolles, executive director, Product Management, Liquid*

#### **Marvell**

“CXL 3.0 will play a significant role in delivering on the promise of fully composable infrastructure for the cloud, bringing increased memory performance and optimal resource utilization to next-generation data centers. CXL is an integral component to Marvell’s industry-leading cloud portfolio which spans compute, electro-optics, memory, networking, security and storage. We applaud the CXL Consortium on this new specification and the ripple-effect it will have in advancing industry innovation.”

*Shalesh Thusoo, VP of CXL Product Development, Marvell*

### **Micron**

“Today’s data centers demand scale, bandwidth and flexibility, and CXL is critical to help meet those needs. As a leading memory and storage provider, we are proud to support the progress of the CXL Consortium. CXL 3.0 builds on the foundation of earlier specifications that help customers address their evolving data center needs, resulting in more workload-optimized system architecture.”

*Raj Hazra, senior vice president and general manager, Micron Compute and Networking business unit*

### **Montage Technology**

“As a CXL Consortium member, Montage Technology is very excited to see the release of the CXL 3.0 specification, which shows how the CXL ecosystem and technology are advancing rapidly towards the next big leap. Leveraging our successful experience in delivering a CXL 2.0 Memory Expander Controller, we will continue to contribute to the consortium development and innovation of the CXL 3.0 technologies and the increasing growth of the CXL ecosystem.”

*Christopher Cox, vice president of Technology, Montage Technology*

### **Numascale**

“Numascale sees the CXL consortium as a key to define the interconnect technology to enable more efficient utilization of compute, memory and storage components for future datacenter architectures. The comprehensive set of features defined in CXL 3.0 address this to enable the industry to develop the components for bringing these new architectures to the market.”

*Einar Rustad, CTO, Numascale*

### **Rambus**

“CXL is a transformative technology that continues to build momentum across the industry. The introduction of CXL 3.0 meets the needs of next-generation data centers with 64 GT/s signaling and a new level of scalability. At Rambus, we are extremely proud to be members of the growing CXL ecosystem and committed to the development of solutions that will accelerate the adoption of this exciting new technology.”

*Travis Karr, general manager of Interconnect SoCs, Rambus*

### **Samsung Electronics**

“With the growth of artificial intelligence, machine learning and cloud computing, Compute Express Link (CXL) is fast becoming critical in addressing the insatiable demand for higher memory density and greater bandwidth. CXL 3.0 opens many doors for technological advancement including peer-to-peer support that can enable direct communication between memory and storage subsystems, in addition to enhanced memory pooling capabilities via fabric-attached memory devices that allow scaling from the node to the rack level. This specification is a milestone that will further the industry’s ability to meet the demands of the Big Data Era, and Samsung looks to continue to collaborate with our ecosystem partners toward mainstream adoption of CXL memory.”

*Cheolmin Park, vice president of the Memory New Business Planning Team, Samsung Electronics, and CXL Consortium Director*

### **SK hynix**

“SK hynix sincerely congratulates the release of CXL 3.0 specification, which will provide robust definitions to realize more advanced and efficient expansion and pooling of CXL memory devices. As we are actively participating in CXL Consortium technical working groups, SK hynix is looking forward to developing more memory features within CXL specification, helping the industry to enable CXL memory

devices as well as expanding their use cases. As a leading memory solution provider, SK hynix is committed to contribute to building CXL ecosystems through novel memories for CXL both in memory expansions and memory pooling. Starting with prototype demos in various events this year, SK hynix will show CXL memory products to the industry, which will be just the beginning toward building scalable and value-added CXL memory solutions in future memory systems.”

*Uksong Kang, vice president of DRAM Product Planning, SK hynix*

### **Synopsys**

“The CXL 3.0 specification’s new capabilities address data-intensive workloads in high-performance computing applications that require greater bandwidth, scalability and security. As an active contributor of the CXL Consortium, Synopsys is already enabling leading customers to integrate the standards-compliant Synopsys CXL 3.0 PHY, controller, IDE security module, and verification IP, helping them get an early start on their advanced chip designs.”

*John Koeter, senior vice president of Marketing and Strategy, Synopsys Solutions Group*

### **Teledyne LeCroy**

“Teledyne LeCroy has worked closely with the CXL Consortium since its inception to align our protocol and physical layer test equipment roadmaps with new generations of CXL specifications. We are excited about continuing this support as the industry moves forward with CXL 3.0 technology providing double the bandwidth by using 64 GT/s data rates and enabling new topology support including fabric and non-tree hierarchies. You can count on us to deliver innovative protocol and physical layer analysis tools to support all stages of development, including silicon, host systems and devices, to enable rapid adoption of this exciting technology.”

*Kevin Prusso, vice president and general manager, Teledyne LeCroy*

### **UnifabriX**

“UnifabriX is harnessing the disruptive power of CXL 2.0 to provide a complete system-level architecture that unleashes exceptional performance and elasticity for the most demanding HPC, AI, and Database workloads above bare-metal and beyond virtualized environments. The evolution of CXL 3.0 towards a native fabric architecture and the introduction of multi-level switching optimize resource provisioning to perfection and enables the rapidly-growing ecosystem of memory-demanding workloads and applications. As a contributing member of the CXL Consortium, UnifabriX is thrilled to unlock the scalability and power of CXL 3.0 fabric interconnects and provide a native transition path to future data-intensive applications.”

*Ronen Hyatt, CEO, UnifabriX*

### **Western Digital**

“Western Digital is pleased to support the release of CXL 3.0 specification. We believe that CXL 3.0 represents a major milestone in the rapidly evolving CXL specification. With its introduction, the promise of memory disaggregation as well as sharing and pooling memory across servers comes closer to reality. Enhanced coherency protocol and direct peer-to-peer communication will enable efficient computational off-load and smart memory subsystems. CXL is driving to become a primary, rack-level system memory interface and presents an exciting opportunity to rethink datacenter architecture. Western Digital is proud to be an active, contributing member of this consortium.”

*Raj Ramanujan, distinguished engineer, Advanced Memory & CXL System Research, Western Digital*

**Wuxi Stars Micro System Technologies Co. Ltd.**

“Wuxi Stars Micro System Technologies Co. Ltd. is focused on Big Data, AI, HPC, and IoT applications. As a pioneer in providing enterprise-level IO expander and high-speed Switch technology solutions, we are excited and proud to be a CXL Consortium Contributor along with the leaders and innovators of the industry. The CXL 3.0 specification doubles the bandwidth while enabling additional usage models such as Memory sharing, Fabric and Multi-level switching. We believe the full potential of CXL 3.0 leads to a rich ecosystem for accelerator, memory, and storage products.”

*Bingquan Huang, technical lead, IP R&D Department 1, Wuxi Stars Micro System Technologies Co. Ltd.*

**Xconn Technologies Holdings Inc.**

“Xconn Technologies is excited to see CXL 3.0 being finalized and released. As a pioneer in CXL switching, Xconn Technologies takes pride as the first silicon provider to bring our CXL 2.0 switch IC to the market, we are working diligently with CXL consortium partner companies to enable CXL ecosystem and memory pooling applications. CXL 3.0 significantly expands the landscape of applications in data center and AI computing. We look forward to continuing our journey and product roadmap by collaborating with the industry to support CXL 3.0.”

*Gerry Fan, president and CEO, Xconn Technologies Holdings Inc.*