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32 Gbps Physical Signaling Specification

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16 November 2020

Approved

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Approved for Distribution to Non-Members for Learning Purposes Only

32 Gbps Physical Signaling Specification

OpenCAPI PHY Signaling Work Group
OpenCAPI Consortium

Version 1.0 (16 November 2020)

Abstract

This document describes the 32 Gbps signaling physical (PHY) layer. This specification focuses on the electrical PHY signaling aspect of the OpenCAPI interface. It is the work product of the OpenCAPI Consortium PHY Signaling Work Group.

This document is handled in compliance with the requirements outlined in the OpenCAPI Consortium Work Group (WG) process document. Comments, questions, etc. can be submitted to membership@opencapi.org.

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Revision log

Each release of this document supersedes all previously released versions. The change history log lists all significant changes made to the document since its initial release. The use of change bars and mark up notation may be included and are noted in the revision log.

Revision date	Summary of changes
16 November 2020	Version 1.0. ● Removed POWER10 references and moved that content into Appendix A. ● Updated acronym table. ● Updated Table 5-1 External Refclk_S_SSC value.
12 June 2020	Version 1.0. This version is the approved version coming out of the PHY Signaling Work Group.
2 April 2020	Version 1.0. This version includes the feedback from the PHY Signaling Work Group.
27 January 2020	Version 1.0. Initial content for submission to the OpenCAPI PHY Signaling Work Group.

About this document

This document describes the 32 Gbps signaling physical (PHY) layer. This specification focuses on the electrical PHY signaling aspect of the OpenCAPI interface.

Note: The IBM® POWER10 processor implements the 32 Gbps PHY. The OpenCAPI columns residing in the tables in this specification are derived from that processor's implementation.

Who should read this document

This specification is intended for designers who plan to develop products that use the OpenCAPI 32 Gbps signaling rate.

Conventions

The OpenCAPI Consortium documentation uses several typesetting conventions.

Notes

This section describes Engineering and Developer notes.

Engineering notes

Engineering notes provide additional implementation details and recommendations not found elsewhere. The notes might include architectural compliance requirements. That is, the text might include Architecture compliance terminology. These notes should be read by all implementation and verification teams to ensure architectural compliance.

Engineering note:

This is an example of an Engineering note. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Proin cursus hendrerit enim, vel tempus nibh ornare ut. Quisque ac augue eu augue convallis hendrerit. Mauris iaculis viverra ipsum nec dapibus. Nunc at porta libero. Curabitur luctus ultrices augue non pulvinar. Vestibulum mattis non ipsum at venenatis. Suspendisse euismod, neque et suscipit luctus, odio metus semper lectus, quis volutpat est libero quis nunc. Vivamus rutrum mauris sed tristique malesuada. Vivamus at augue vitae nisl cursus feugiat.

Developer notes

Developer notes are used to document the reasoning and discussions that led to the current version of the architecture. These notes might also include recommended changes for future versions of the architecture, or warnings of approaches that have failed in the past. These notes should be read by verification teams and contributors to the architecture.

Developer note:

This is an example of a Developer note. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Proin cursus hendrerit enim, vel tempus nibh ornare ut. Quisque ac augue eu augue convallis hendrerit. Mauris iaculis viverra ipsum nec dapibus. Nunc at porta libero. Curabitur luctus ultrices augue non pulvinar. Vestibulum mattis non ipsum at venenatis. Suspendisse euismod, neque et suscipit luctus, odio metus semper lectus, quis volutpat est libero quis nunc. Vivamus rutrum mauris sed tristique malesuada.

Terms

The following terms are used in this document.

AC	Alternating current
AIC	Add-in card
ASIC	Application-specific integrated circuit
BER	Bit error rate
BUJ	Bounded uncorrelated jitter
BW	Bandwidth
CAPI	Coherent Accelerator Processor Interface
CDM	Charge device model
CDR	Clock data recovery
CEI	Common electrical I/O
CM	Common mode
CPU	Central processing unit
CRC	Cyclic redundancy check
CTLE	Continuous time linear equalizer
DC	Direct current
DCD	Duty Cycle Distortion
DDJ	Data-dependent jitter
DL	OpenCAPI data link layer on the host processor
FEXT	Far-end cross talk
FFE	Feed-forward equalizer
FPGA	Field-programmable gate array
Gbps	Gigabits per second
GHz	Gigahertz
GPU	Graphics processing unit
Gsym/s	Giga symbols per second
HBM	Human body model

HPF	High-pass filter
HSSCDR	High-speed SerDes/clock data recovery
ILD	Insertion loss deviation
JEDEC	Joint Electron Device Engineering Council
JTOL	Jitter tolerance
LFEQ	Low-frequency equalizer
LGA	Land grid array
MR	Medium reach
NEXT	Near-end cross talk
NRZ	Non-return-to-zero
OIF	Optical Internetworking Forum
PCB	Printed circuit board
PHY	The physical (PHY) layer interfaces to the DL and the network. This is the bit stream level that specifies the electrical and optical transmission medium as well as the network interconnect topology. The current specification for the network is a point-to-point connection.
PLL	Phase-locked loop
RJ	Random jitter
RMS	Root mean square
RX	Receiver
SerDes	Serializer/de-serializer
SR	Short reach
SRIS	Separate Refclk Independent Spread
SSC	Spread spectrum clocking
SST	Source series terminated
TJ	Total jitter

TL	OpenCAPI transaction layer found on the host processor. Interfaces to the DL and the protocol layer. response-packet handling and formation. Ensures that the order of data sent to the DL matches the command and response packet order sent to the DL. Manages data flits from the DL and associates the data with the command or response packet that was received prior to the arrival of the data. The command and response packets contain data descriptors that enable this association. Provides flow control. Provides error handling and control. Manages virtual channels, virtual queues, and service queues associated with the virtual channels. Order is retained within virtual channels.
TX	Transmitter
UBHPJ	Uncorrelated bounded high-probability jitter
UIPP	Unit interval peak-to-peak
UUGJ	Uncorrelated unbounded Gaussian jitter
VCM	Voltage common mode
VNA	Vector Network Analyzer

1. Overview

This document describes the OpenCAPI 32 Gbps signaling physical (PHY) layer. Note that in regard to OpenCAPI, any high-speed PHY can accommodate this protocol. However, following this specification enables a device to interface and support the OpenCAPI protocol, which uses this interface during communication between devices; including, but not limited to accelerators, memory and advanced memory solutions, GPUs, CPUs, signal repeaters, and so on. This specification is focused on the electrical PHY signaling aspect of the OpenCAPI interface. If a hardware IP meets both the over-clocked OIF CEI-28G-MR specification running at 32 Gbps, as well as the PCIe Gen5 specifications at 32Gbps, then in principle the IP will be compliant to the OpenCAPI 32 Gbps PHY specifications.

2. Channel description

The 32 Gbps PHY is a medium-reach channel, chip-to-chip differential interface that provides data links between the following components: GPU-to-CPU, CPU-to-CPU, cable connections such as on-board and with half-active cables, and CPU-to-FPGA for CAPI acceleration (or any other types of end points or ASICs). The interface is a striped serial design (multiple lanes in parallel defining the bus width). Each lane is required to perform clock data recovery (CDR) and there is no clock forwarding.

3. Channel highlights

The medium-reach, chip-to-chip interface features include:

- A 30 dB insertion loss support at the Nyquist frequency (die-to-die, or bump-to-bump, or c4-to-c4)
- PCB or Passive copper cables
- See the *32 Gbps Interface Mechanical Specification* for details for the CPU complex (substrate trace to on the substrate pad) and Advance Accelerator socket/package etc. insertion loss budgets

3.1 I/O protocol

I/O protocol features include:

- 32 Gbps (133.33 MHz reference clock for JEDEC applications) and
  31.875 Gbps (156.25 MHz reference clock for over-clocked OIF applications).
- Differential signaling with termination
- NRZ
- Scrambled
- DC or externally AC coupled
- Link configuration: unidirectional lanes upstream and downstream

3.2 Reference clock

The reference clock is an external, 133.33 MHz or 156.25 MHz crystal clock distributed (32 Gbps → 133.33 MHz reference clock, or 31.875 Gbps → 156.25 MHz reference clock) on the PCB. For drawer-to-drawer, the reference clock is not required to be forwarded. The data link layer (DL) handles clock compensation and includes 64/66 encoding. Planar synchronous reference clocks can also be used. For a separate reference clock design, see the *Optical Internetworking Forum (OIF) CEI-28G-MR Specification*.

3.3 Link perspective

The channel is constructed from the endpoint PHY; the module package/substrate wiring and c4 (die pad); the card/planar wiring, connectors; and the module package/substrate wiring, c4 (die pad), and socket. From a system perspective, the channel is used to establish a communication link between the endpoint logic functions and OpenCAPI 32 Gbps compliant processor logic functions.

This section of the specification does not provide the following link-level information.

3.3.1 Link power states

Link power states are defined in the *OpenCAPI Data Link Layer (DL 3.0/3.1/4.0) Architecture Specification*.

3.3.2 Training sequence

The *OIF CEI-28G-MR Specification* defines a thin PHY that does not include thick PHY functions such as: bit-lane repair, deskew, scrambler/descramble, and so on. In addition to the thick PHY functions, the link layer

is responsible for the CRC insertion/checking, replay buffers, and link layer retry protocols.

3.3.3 Data link layer (DL)

This design uses 64/66 encoding, scrambling, and framing. See the *OpenCAPI Data Link Layer (DL3.0/3.1/4.0) Architecture Specification* for details.

4. Channel definition

4.1 Channel requirements

The channel includes an end-to-end link. It consists of bump capture pads, a package including balls, LGA modules, PCB route, connectors, sockets, and other physical media between the driver and receiver. It does not include on-die termination. *Table 4-1* lists the channel requirements.

Note: IBM uses an internal tool called HSSCDR to model the total channel with full aggressors. Channel models are available from *drepsdm@us.ibm.com*.

Table 4-1. Channel requirements

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
$T_{CH\_SKEW\_Host\_RX}$	Delay difference between lanes within a bundle when a GPU/ASIC/FPGA is driving to the 32 Gbps PHY compliant processor. **Note:** bundle = x4, x8, x16 (port width).			132	UI	Skew between lanes is inclusive of on-chip consumption. Maximum skew of TX is 64 UI from end-point input. DL layer should be designed to handle 132 UI.
$T_{CH\_SKEW\_Host\_TX}$	Delay difference between lanes within a bundle driven from the 32 Gbps PHY compliant processor, launch skew, board and package skew, and retime skew			12.5	UI	Skew between lanes inclusive with 1.6 UI allocated to cables. The 12.5 UI budget is equivalent to 390 ps total budget for a 32 Gbps data rate. The 12.5 UI budget covers the passive channel design between the dies (and not the dies themselves). The system die-to-die, lane-to-lane skew should meet this number.
IL(f)	Channel insertion loss at Nyquist frequency			30	dB	PHY maximum loss capability from die-to-die (c4-to-c4). Includes PCB manufacturing variations and tolerance including the effects of humidity and temperature variations on dielectric materials. The maximum PCB loss should be this number minus the losses of the host plus endpoint chip package. Insertion loss for a channel must be quantified with a 42.5 Ω port reference impedance/85 Ω differential.

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
ILD(RMS)	Measure of deviation from the insertion loss curve within a specified frequency range			0.45	dB RMS	This is the RMS value of discrete frequency point errors between the insertion loss curve and insertion loss curve fit. The insertion loss curve is found using a moving average smoothing (1GHz window size). See *Section 4.2 Insertion loss deviation measure [ILD(RMS)] calculation* and *Section 4.3 Moving-average smoothing* for additional details. Insertion loss used for a channel must be quantified with a 42.5 Ω port reference impedance.
NEXT(f)	Power sum NEXT at Nyquist frequency			-55	dB	Calculated by carrying out the root sum square of all NEXT aggressors onto the victim differential pair. All channels must be designed so that FEXT is the dominant source of crosstalk. TX/RX PCB wiring must be done on different layers or TX/RX pin and via combinations must have sufficient ground isolation. NEXT Power Sum for a channel must be quantified with a 42.5 Ω port reference impedance.
FEXT(f)	Power sum FEXT at Nyquist frequency			-48	dB	Calculated by carrying out the root sum square of all FEXT aggressors onto the victim differential pair. FEXT Power Sum for a channel must be quantified with a 42.5 Ω port reference impedance.
ICR	Insertion loss to cross talk ratio at Nyquist frequency	18			dB	Difference between insertion loss and crosstalk power-sum value. Also known as signal-to-crosstalk ratio.
$TEMP_{CH}$	Temperature	0		100	°C	Ambient temperature of channel.
RL_{CH_DIFF}	Differential return loss at Nyquist	10			dB	Optimally, the minimum differential return loss between 0 Hz and Nyquist occurs at Nyquist. This rule can be broken if simulations show passing eye margins. See *Section 5.6.4 Differential return loss for both transmitter and receiver.* Return loss for a channel must be quantified with a 42.5 Ω port reference impedance.
RL_{CH_CM}	Common mode return loss at Nyquist	10			dB	Optimally, the minimum common-mode return loss between 0 Hz and the Nyquist frequency occurs at the Nyquist frequency. Return loss for channel must be quantified with 42.5 Ω port reference impedance.
Z_{CH_DIFF}	Differential impedance	-10%	85	+10%	Ω	Channel impedance. **Note:** This deviates from the OIF CEI-28G-MR, which is ±100 Ω.

4.2 Insertion loss deviation measure [ILD(RMS)] calculation

To quantify insertion loss deviation [ILD(RMS)] measure, a fit of the insertion loss magnitude curve (in dB) is generated between 1 GHz and 20 GHz. The curve fitting of the insertion loss is done by a moving average smoothing procedure. The moving average smoothing procedure assumes a window size of 1 GHz centered at the point under consideration. After a fitted line is obtained, the error between the original insertion loss curve and the fitted curve is found at each discrete frequency point in the S-parameter model. The square of each discrete frequency point error is then found after which it is scaled by the magnitude of the FFT of a 32 Gbps rectangular pulse having 900 mVpk amplitude at the corresponding frequency points. The sum of all scaled squared discrete frequency point errors is calculated and divided by the total number of discrete frequency points considered. The square root of the resulting value is ILD(RMS).

4.3 Moving-average smoothing

The following steps describe the moving-average smoothing procedure:

1. Select the size of the window of the moving average to be 51 discrete points. This window spans a 1 GHz range with 20 MHz steps.

2. For each discrete frequency point, beginning with the 26th discrete point and ending with the highest_frequency_point_minus_25, find the average of all the values ranging between the 25 values before the considered point and the 25 values after the considered point.

3. For each discrete frequency point between the first and the 25th point, find the average of all values between all the lower frequency points and as many frequency points higher than the considered point.

4. For each discrete frequency point between the 25th point-to-the-last and the last, find the average of all the values between all of the higher frequency points and as many frequency points lower than the considered point.

5. Generate a smoothed curve of the insertion loss using the averages calculated in steps 2, 3, and 4 at each frequency point.

5. Electrical specifications

5.1 Power supply

Any required endpoint power supplies are handled at the system design level. For AC-coupled PHYs, the endpoint power supply is not specified. For DC-coupled PHYs, the V_{CM} must satisfy the host V_{CM} range.

5.2 External reference clock

External reference clock system design is common clocking and is allowed with down spread. *Table 5-1* lists the external reference clock specifications.

Table 5-1. External reference clock specification

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
ref_clk	Reference clock frequency and tolerance	-30 ppm	156.25	30 ppm	MHz	Over-clocked OIF application
		-30 ppm	133.33	30 ppm	MHz	JEDEC application
L_100K	Phase noise at 100 kHz from carrier		-120		dBc/Hz	
JIT_{REFCLK}				1	ps RMS	Integrated over 1 kHz – 20 MHz.
S_SSC	SSC (optional) spread	-2000		0	ppm	This is for a common clock-based spread. If the endpoints do not have the same oscillator, spread cannot be invoked. System design requires a common clock with possible down spread. Steps are -1000, -2000 ppm.
FM_SCC	Modulation frequency	30		33	kHz	
T_{REFCLK}	Routing delay between RX/TX			10	ns	Insertion delay between chips.
$VDIFF_{REFCLK}$	Differential voltage swing	0.575		0.85	V_{PPD}	
VCM_{REFCLK}	Common mode	0.35		0.4	V	
F_{AC_REFLCK}	AC coupling (required)			10	kHz	AC coupling HPF corner.
TR_{REFCLK}	Rise/fall time	0.2		1	ns	*Figure 5-3. 20% - 80% rise/fall time calculation.*
Z_{DIFF_REFLCK}	Differential impedance	-10%	85	+10%	Ω	

Table 5-2. Data rate independent reference clock parameters

Symbol	Description	OpenCAPI	Units	Notes
F_{REFCLK}	Reference clock frequency	133.33 ±30 ppm	MHz	1
		156.25 ±30 ppm	MHz	1
F_{SSC}	SSC frequency range	30 (minimum), 33 (maximum)	kHz	1
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.2 (minimum), 0 (maximum)	%	1, 2
$T_{SSC-FREQ-DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 Gbps and SRIS when operating in SRIS mode at all speeds	NA	%	1, 2

Notes:

1. OpenCAPI runs in common clock mode only.
2. OpenCAPI is only applied in a server environment; therefore, in OpenCAPI, -2000 ppm SSC is acceptable. This is common spread.

5.2.1 Tx and Rx PLLs

Table 5-3 provides a reference (or informative) specification of the TX and RX phase locked loop circuits in a common-clock (or Common Reference Clock) system. This serves as a guide for other architectures, implementations, or designs.

Table 5-3. TX and RX PLLs, informative specification

Symbol	Description	Minimum	Maximum	Unit	Description	Notes
BW_{PLL}	TX and RX PLL bandwidths	0.5	1.8	MHz	Second-order PLL jitter transfer bounding function.	1, 2
PKG_{PLL}	TX and RX PLL peakings	N/A	2.0	dB	Second-order PLL jitter transfer bounding function.	1, 2

Notes:

1. A single combination of PLL bandwidth and peaking is specified for 32.0 Gbps implementations. For other data rates, two combinations of PLL bandwidth and peaking are specified to permit designers to make a tradeoff between the two parameters.
2. The TX PLL bandwidth must lie between the minimum and maximum ranges given in the table. PLL peaking must lie below the value listed. The PLL bandwidth extends from zero up to the value(s) specified in the table. The PLL bandwidth is defined at the point where its transfer function crosses the -3 dB point.

5.3 I/O lane

Table 5-4 lists the electrical specification for TX and RX terminations.

Table 5-4. Electrical specification for TX[1] and RX termination

Symbol	Description	Minimum	Typical	Maximum	Unit	Notes
Z_{DIFF_IO}	Differential impedance	-10%	85	+10%	Ω	Impedance during normal mode and idle mode.
Z_{SE_IO}	Single-ended impedance		42.5		Ω	The two single-ended resistances must match within 5%.
$dV_{GND,TxRx}$	Ground difference			50	mV_{PP}	Ground differences between TX and far-end RX.
ILIO	Bandwidth or loss due to poles		-1	-1.5	dB	A total budget of 3 dB for (TX and RX) should be accounted for in the link budget.
RL_{DIFF_IO}	Differential return loss				dB	See *Figure 5-5. SDD11 and SDD22 differential return loss at c4 (pads) template for RX and TX (from OIF CEI-28G-MR Specification)* for more information.
RL_{CM_IO}	Common-mode to differential and differential to common-mode				dB	See *Figure 5-7. SDC11 and SCD11 for module input (TP1) and host input (TP4a) (for fb = 32 GHz)* for more information.

Notes:

1. The OpenCAPI TX must be designed to have minimum FFE capability of one precursor and one main cursor with 1 UI span per cursor. The precursor must at least have 0% - 15% coefficient setting range capability. This minimum FFE capability in the transmitter should be sufficient as long as good receiver equalization is available.

5.4 Data rate dependent parameters

Table 5-5. Data rate dependent transmitter parameters

Symbol	Description	32.0 Gbps	OpenCAPI	Units	Notes
UI	Unit interval	31.246875 (minimum) 31.253125 (maximum) (±100 ppm)	31.249063 (minimum) 31.250938 (maximum) (±30 ppm)	ps	Does not include SSC variations.
$V_{TX-DIFF-PP}$	Differential peak-peak TX voltage swing for full-swing operation	800 - 1300	800 - 1300	mV_{PP}	As measured with compliance test load. Defined as 2*|VTXD+ - VbTXD-|. See note 1.
$ps21_{TX-ROOT-DEVICE}$	Pseudo package loss of a device containing root ports	8.5 (maximum)	8.5 (maximum)	dB	See note 2.
$ps21_{TX-NON-ROOT-DEVICE}$	Pseudo package loss for all devices not containing root ports	3.7 (maximum)	3.7 (maximum)	dB	See note 2.
$ILfit_{TX-ROOT-DEVICE}$	Fitted insertion loss at Nyquist	9.0 (maximum)	9.0 (maximum)	dB	See note 3.
$ILfit_{TX-NON-ROOT-DEVICE}$	Fitted insertion loss at Nyquist	4.0 (maximum)	4.0 (maximum)	dB	See note 3.
$V_{TX-BOOST-FS}$	Maximum nominal TX boost ratio for full swing	8.0 (minimum)	8.0 (minimum)	dB	Nominal boost beyond 8.0 dB is limited to guarantee that ps21TX limits are satisfied.
$EQ_{TX-COEFF-RES}$	TX coefficient resolution	1/63 (minimum) 1/24 (maximum)	Larger steps allowed	N/A	
T_{TX-UTJ}	TX uncorrelated total jitter	6.25 (maximum)	6.25 (maximum)	ps PP at 10^{-12}	See *Figure 5-2. Derivation of TTX-UTJ and TTX-UDJDD*.
$T_{TX-UDJDD}$	TX uncorrelated deterministic jitter (dual-Dirac model) for non-embedded refclk	3.125 (maximum)	3.125 (maximum)	ps PP	See *Figure 5-2. Derivation of TTX-UTJ and TTX-UDJDD*.
$T_{TX-UPW-TJ}$	TX Total uncorrelated pulse width jitter	6.25 (maximum)	6.25 (maximum)	ps PP at 10^{-12}	See *Figure 5-6. TX, RX differential return loss mask with 42.5 Ω* reference.
$T_{TX-UPWDJDD}$	TX uncorrelated deterministic pulse width jitter (dual-Dirac model)	2.5 (maximum)	2.5 (maximum)	ps PP	See *Figure 5-6. TX, RX differential return loss mask with 42.5 Ω* reference.
$L_{TX-SKEW}$	Lane-to-lane output skew	1.25 (maximum)	1.25 (maximum)	ns	Between any two lanes within a single transmitter.
$RL_{TX-DIFF}$	TX package plus die differential return loss	See *Figure 5-6. TX, RX differential return loss mask with 42.5 Ω reference*.	See *Figure 5-6. TX, RX differential return loss mask with 42.5 Ω reference*.	dB	

Symbol	Description	32.0 Gbps	OpenCAPI	Units	Notes
RL_{TX-CM}	TX package plus die common-mode return loss	See *Figure 5-8. TX, RX common mode return loss mask with 42.5 Ω reference*	See *Figure 5-8. TX, RX common mode return loss mask with 42.5 Ω reference*	dB	

Notes:

1. See *Section 8.3.3.7 Method for Measuring VTX-DIFF-PP at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s* in the *PCIe 5.0 Specification*.
2. The numbers account for measurement error. For some TX package/driver combinations, ps21TX may be greater than 0 dB.
3. These are design parameter requirements; a specific test methodology for them is not defined.

Figure 5-1. PWJ relative to consecutive edges 1 UI apart

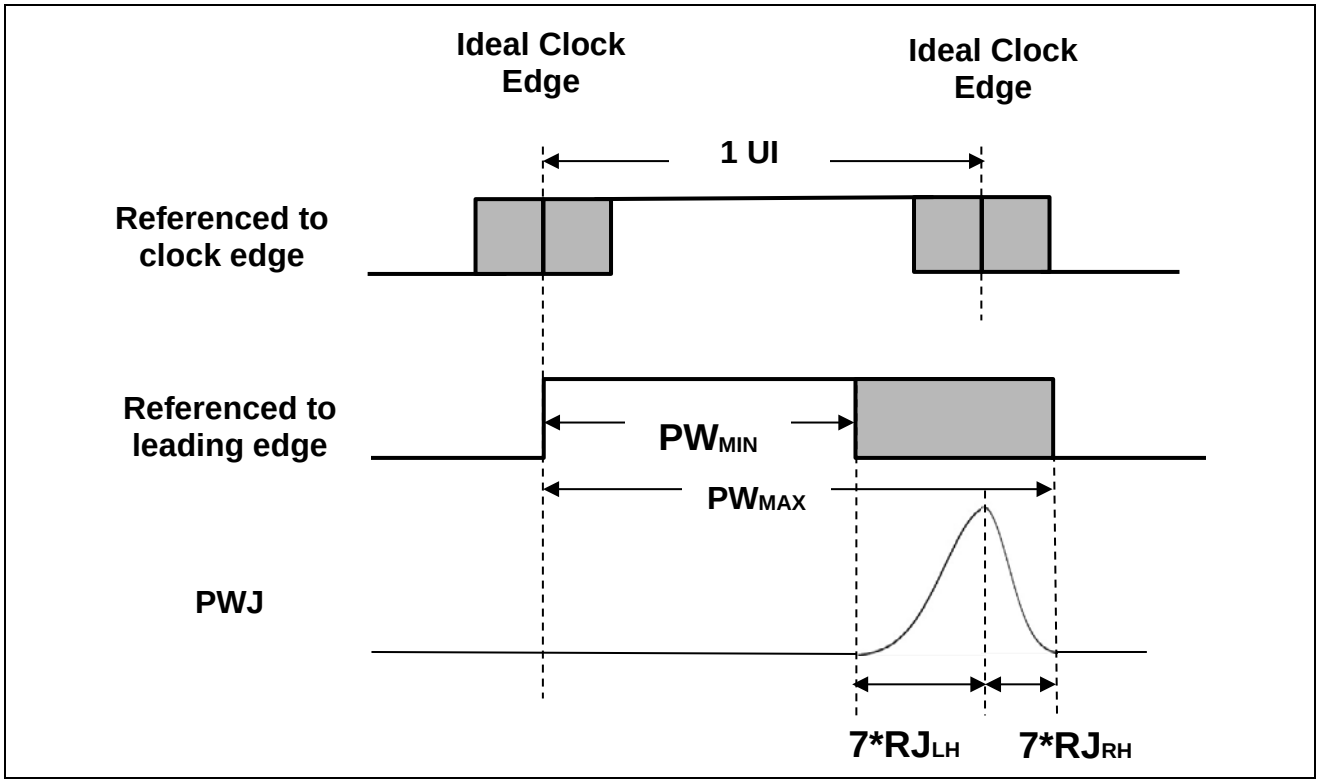
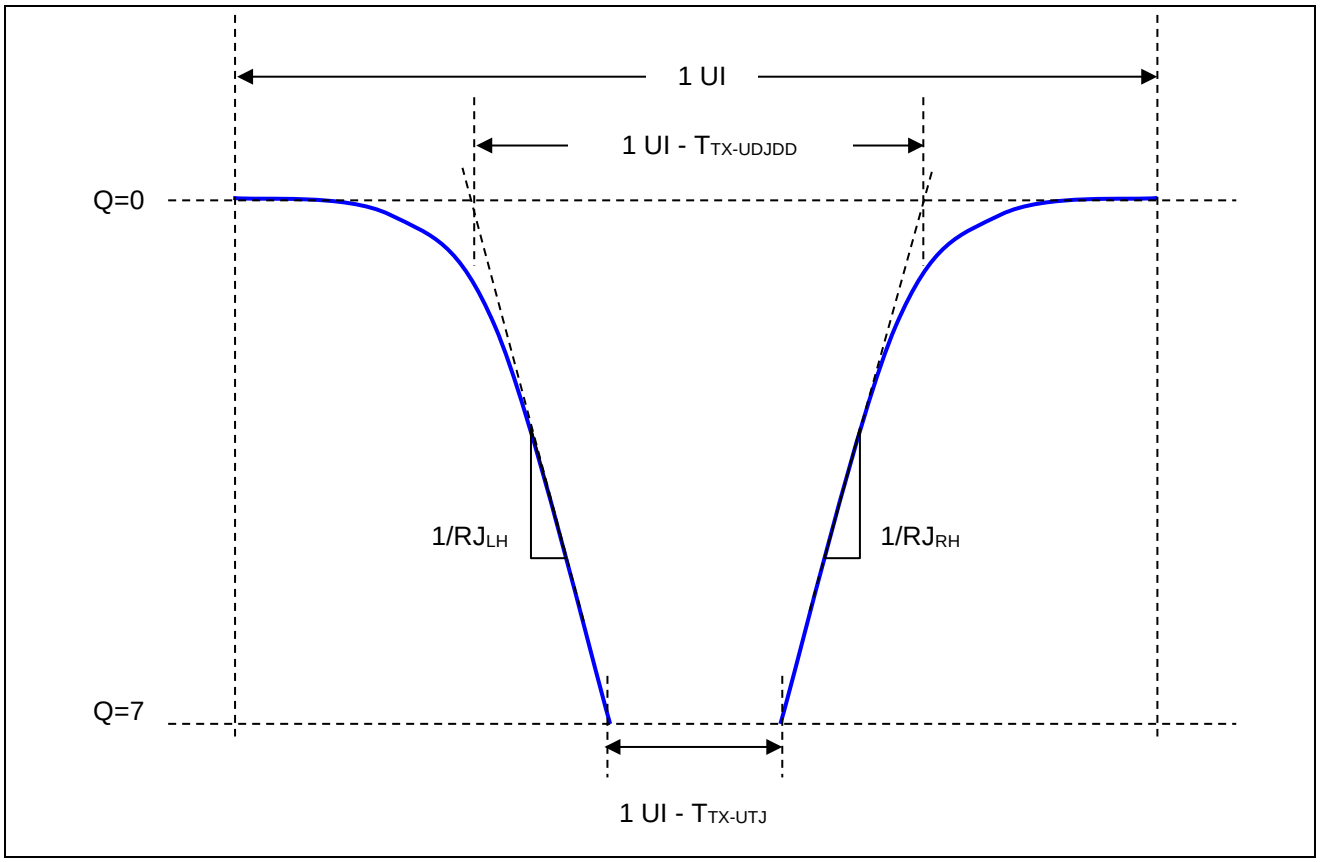


Figure 5-2. Derivation of T_{TX-UTJ} and $T_{TX-UDJDD}$



5.5 Data rate independent parameters

Table 5-6 describes the data rate independent transmitter parameters.

Table 5-6. Data rate independent transmitter parameters

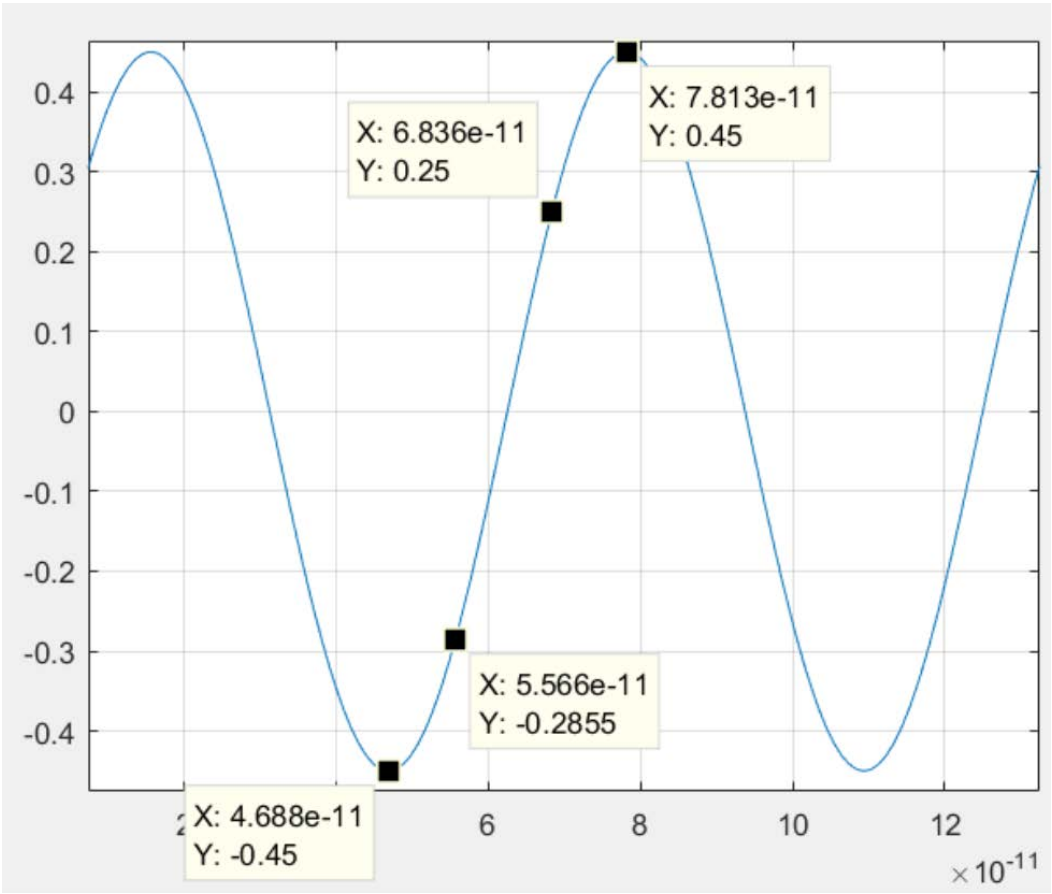
Symbol	Description	32.0 Gbps	OpenCAPI	Units	Notes
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	TX AC peak-peak common-mode voltage	150 (maximum)	150 (maximum)	mV_{PP}	Over the 0.03 - 500 MHz range: no more than 100 mV_{PP} at 32.0 Gbps. See note 2.
$V_{TX\text{-}DC\text{-}CM}$	TX DC peak-to-peak common-mode voltage	0 (minimum) 3.6 (maximum)	0 (minimum) 3.6 (maximum)	V	Total single-ended voltage a TX can supply under any conditions with respect to ground. See also the $I_{TX\text{-}SHORT}$. See note 1.
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 (minimum) 25 (maximum)	0 (minimum) 25 (maximum)	mV	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-\ [during\ L0]} \rvert \leq 25\ mV$ $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} \rvert$ [during L0] $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-} \rvert$ [during L0]
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}p}$	Electrical idle differential peak output voltage	0 (minimum) 20 (maximum)	N/A	mV	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}p} = \lvert V_{TX\text{-}Idle\text{-}D+} - V_{Tx\text{-}Idle\text{-}D-} \rvert \leq 20\ mV.$ Voltage must be band-pass filtered to remove any DC component and HF noise. The bandpass is constructed from two first-order filters, the high-pass and low-pass 3 dB bandwidths are 10 kHz and 1.25 GHz, respectively.
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during receiver detection	600 (maximum)	N/A	mV	The total amount of voltage change in a positive direction that a transmitter can apply to sense whether a low-impedance receiver is present. Note: Receivers display substantially different impedance for $V_{IN} < 0$ versus $V_{IN} > 0$.
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	20 (minimum)	N/A	ns	The time a TX must spend in Electrical Idle before transitioning to another state.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid diff signaling after leaving electrical idle	8 (maximum)	N/A	ns	Maximum time to transition to valid diff signaling after leaving electrical idle. This is considered a debounce time to the TX.
$T_{CROSSLINK}$	Crosslink random timeout	1.0 (maximum)	N/A	ms	This random timeout helps resolve potential conflicts in the crosslink configuration.
C_{TX}	AC coupling capacitor	176 (minimum) 265 (maximum)	176 (minimum) 265 (maximum)	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. Recommended to use 0201 capacitor.

Symbol	Description	32.0 Gbps	OpenCAPI	Units	Notes
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	120 (maximum)	120 (maximum)	Ω	Low impedance defined during signaling. The minimum value is bounded by $RL_{TX\text{-}DIFF}$. Must also meet launch voltage $V_{TX\text{-}DIFF\text{-}PP}$.
$I_{TX\text{-}SHORT}$	TX short circuit current	90 (maximum)	90 (maximum)	mA	TX short-circuit current. See note 1.

Notes:

1. $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst-case transients that a receiver must tolerate.
2. $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM only and is not intended to capture system CM noise. For each data rate, an LPF with a -3 dB point of data rate/2 is applied.

Figure 5-3. 20% - 80% rise/fall time calculation



Note: 20% - 80% rise/fall time has been calculated using a sine wave with the half period being 31.25 ps (1 UI at 32 Gbps) as shown in *Figure 5-3*.

5.5.1 Electrical output specification

Table 5-7 shows the endpoint transmitter electrical output specification and is based on an over-clocked *OIF CEI-28G-MR Specification* but with the maximum baud rate increased to 32.0 Gsym/s.

Table 5-7. Endpoint transmitter electrical output specification

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit	Comment
T_Baud	Baud rate		19.90		32.0	Gsym/s	
T_V_{DIFF}	Output differential voltage	Emphasis off. See Note 1.	800		1200	mV_{PPD}	PCIe is 1300 mV maximum.
T_V_{SE}	Single-ended transmitter output voltage		-0.3		1.9	V	
T_R_{D}	Differential resistance	Channels are designed 85 Ω (see note 2).	80	100	120	Ω	
T_R_{DM}	Differential termination resistance mismatch				10	%	See *the OIF CEI-28G-MR Specification*.
T_tr, T_tf	Output rise and fall time (20% - 80%)	Emphasis off. See Note 3.	8		12.7 (maximum)	ps	6.875 at 32 Gbps
T_N_{CM}	Common-mode noise	See Note 1.			12	mV_{RMS}	Need to also meet the PCIe specification.
T_SDD22	Differential output return loss	See *Section 5.6.4 Differential return loss for both transmitter and receiver*				dB	
T_SCC22	Common-mode output return loss	Below 10 GHz			-6	dB	PCIe @ 32 Gbps is -3 dB
		10 GHz to baud rate			-4		
T_V_{CM}	Output common-mode voltage	Load Type 0 See note 4.	-100		1700	mV	AC coupling capacitor is required. See C_{TX} in *Table 5-6. Data rate independent transmitter parameters*

Notes:

1. The procedure is defined in *Section* 5.7. *Characterizing channel common mode noise*.
2. Nominal 85 Ω channels are designed from c4-to-c4. Endpoint package traces of the endpoint module should also be defined to be 85 Ω. If the endpoint is 100 Ω in the silicon and the package is 100 Ω, regression is required to ensure that the ILD is acceptable.
3. The transmitter-under-test is preset such that C0 is its maximum value (C0_max) and all other coefficients are zero. The 20% and 80% values are of the steady state one and zero. The maximum value is limited by meeting the transmit launch through loss (s12) of 0 dB.
4. Load type 0 is AC coupled. The AC coupling capacitors exist near the endpoint devices.

5.5.2 TX jitter models

The following jitter terms are specified at the PAD or c4 of the chip. The carrier organic package is considered part of the channel. TX silicon S-parameter models are available upon request. The TX jitter test methods follow the PCIe5 methods.

Table 5-8. Transmitter output jitter specification

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit	Comment
T_UUGJ	Uncorrelated unbounded gaussian jitter				0.15	UIPP	Need to meet the PCIe jitter decomposition.
T_UBHPJ	Uncorrelated bounded high-probability jitter (UBHPJ)	Note 2			0.15	UIPP	
T_EOJ	Even-odd jitter (component of UBHPJ)	Note 3			0.035	UIPP	
T_TJ	Total jitter	Note 1			0.20	UIPP	If greater than 0.20, it must be handled on a case-by-case basis.

Notes:

1. T_TJ includes all of the jitter components measured without any transmit equalization.
2. Measured with all possible values of transmitter equalization, excluding DDJ, as defined in *Section 6.2 Data dependent jitter (DDJ) measurement*. Included in T_UBHPJ, even-odd jitter is measured on two repetitions of a repeating pattern with an odd number of bits and at least two transitions between one and zero or zero and one. PRBS9 is such a pattern. The deviation of the time of each transition from an ideal clock at the signaling rate is measured. Even-odd jitter is defined as the magnitude of the difference between the average deviation of all even-numbered transitions and the average deviation of all odd-numbered transitions, but only actual transitions are measured and averaged. Note: Even-odd jitter has been referred to as duty cycle distortion (DCD) by other CEI specifications.
3. Measured with all possible values of transmitter equalization.

The TX jitter test methods follow the CEI-28G-MR test methods. *Table 5 -6 Transmitter output jitter specification for endpoint* (from the *OIF CEI-28G-MR Specification*) can be used for the jitter parameters to simulate the transmitter.

T_UUGJ is specified for BER 1e-15 for over-clocked OIF applications

T_UUGJ is specified for BER 1e-12 for PCIe applications

5.6 Endpoint receiver

5.6.1 Common receiver parameters

Table 5-9 lists the common receiver parameters that are not directly associated with stressed eye tolerancing.

Table 5-9. Common receiver parameters

Symbol	Description	32.0 Gbps	OpenCAPI	Units	Notes
UI	Unit interval	31.246875 (minimum) 31.253125 (maximum) (±100 ppm)	31.246875 (minimum) 31.253125 (maximum) (±30 ppm)	ps	UI tolerance does not include SSC effects.
$RL_{RX-DIFF}$	Differential receiver return loss	See *Figure 5-6. TX, RX differential return loss mask with 42.5 Ω reference*	See *Figure 5-6. TX, RX differential return loss mask with 42.5 Ω reference*	dB	See Note 1.
RL_{RX-CM}	Common mode receiver return loss	See *Figure 5-8. TX, RX common mode return loss mask with 42.5 Ω reference*	See *Figure 5-8. TX, RX common mode return loss mask with 42.5 Ω reference*	dB	See Note 1.
$V_{RX-CM-AC-P}$	RX AC common mode voltage	75 (max) for EH < 100 mV_{PP} 125 (max) for EH ≥ 100 mV_{PP}	75 (max) for EH < 100 mV_{PP} 125 (max) for EH ≥ 100 mV_{PP}	mV_{PP}	Measured at RX pins into a pair of 42.5 Ω terminations to ground.
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V ≥ 0 during reset or power-down	≥10 K (0 - 200 mV ≥20 K (> 200 mV)	≥10 K (0 - 200 mV ≥20 K (> 200 mV)	Ω	Voltage measured with respect to ground. Parameters might not scale with process technology. See Note 2.
$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power-down	1.0 K (minimum)	1.0 K (minimum)	Ω	Parameters might not scale with process technology. See Note 2.
$L_{RX-SKEW}$	Lane-to-lane skew	5 (maximum)	5 (maximum)	ns	Across all lanes on a port. $L_{RX-SKEW}$ comprehends lane-to-lane variations due to channel and repeater delay differences.

Notes:

1. Measurements must be made for both common mode and differential return loss. In both cases, the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.
2. $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined respectively for negative and positive voltages at the input of the receiver. Transmitter designers must comprehend the large difference between >0 and <0 RX impedances when designing receiver detect circuits.

5.6.2 Electrical input specification

Table 5-10 describes the endpoint receiver electrical input specification and is essentially the same as the *OIF CEI-28G-MR Specification* except for the differential input impedance and the maximum baud rate increased to 32.0 Gsym/s.

Table 5-10. Endpoint receiver electrical input specifications

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit	Comment
R_Baud	Baud rate		19.90		32.0	Gsym/s	
R_V_{DIFF}	Input differential voltage	See note 1.			1200	mV_{PPD}	
R_Rd_{IN}	Differential input impedance		80	100	120	Ω	
R_R_M	Input impedance mismatch				10	%	
R_SDD11	Differential input return loss	*Refer to Table 1-9.* Differential return loss for both transmitter and receiver.					PCIe @ 32 Gbps is -6 dB.
R_SCC11	Common mode input return loss	Below 10 GHz.			-6	dB	PCIe @ 32 Gbps is -3 dB.
		10 GHz to baud rate.			-4		
R_V_{CM}	Input common mode voltage	Load type 0. See note 2.	-150		1750	mV	AC coupled OIF.

Notes:

1. The receiver shall have a differential input voltage range sufficient to accept a signal produced at point R by the combined transmitter and channel. The channel response shall include the worst-case effects of the return losses at the transmitter and receiver.
2. Load Type 0 with minimum T_V_{DIFF}, AC coupling or floating load. For floating load, input resistance shall be 1 KΩ. Only applies if AC-coupling capacitor is integrated in the receiver.

Table 5-11. Receiver input jitter specification (from OIF CEI-28G MR Specification)

Symbol	Characteristic	Condition	Minimum	Typical	Maximum	Unit	Comment
R_SJ-max	Sinusoidal jitter, maximum	Receiver compliance Section *of* the *OIF CEI-28G-MR Specification.* See note 1.			5	UI_{PP}	See *Figure 5-4. Sj Mask for Receivers Operating in Common Clock mode at 32.0 Gbps*.
R_SJ-hf	Sinusoidal jitter, high frequency	Receiver compliance Section *of* the *OIF CEI-28G-MR Specification.* See note 1.			0.10	UI_{PP}	

Notes:

1. The receiver must tolerate the sum of these jitter contributions: total transmitter jitter from *Table 1-6 on page 18*; sinusoidal jitter as previously defined; and the worst-case effects of a channel that is compliant to the channel characteristics

5.6.3 Stressed jitter eye parameters

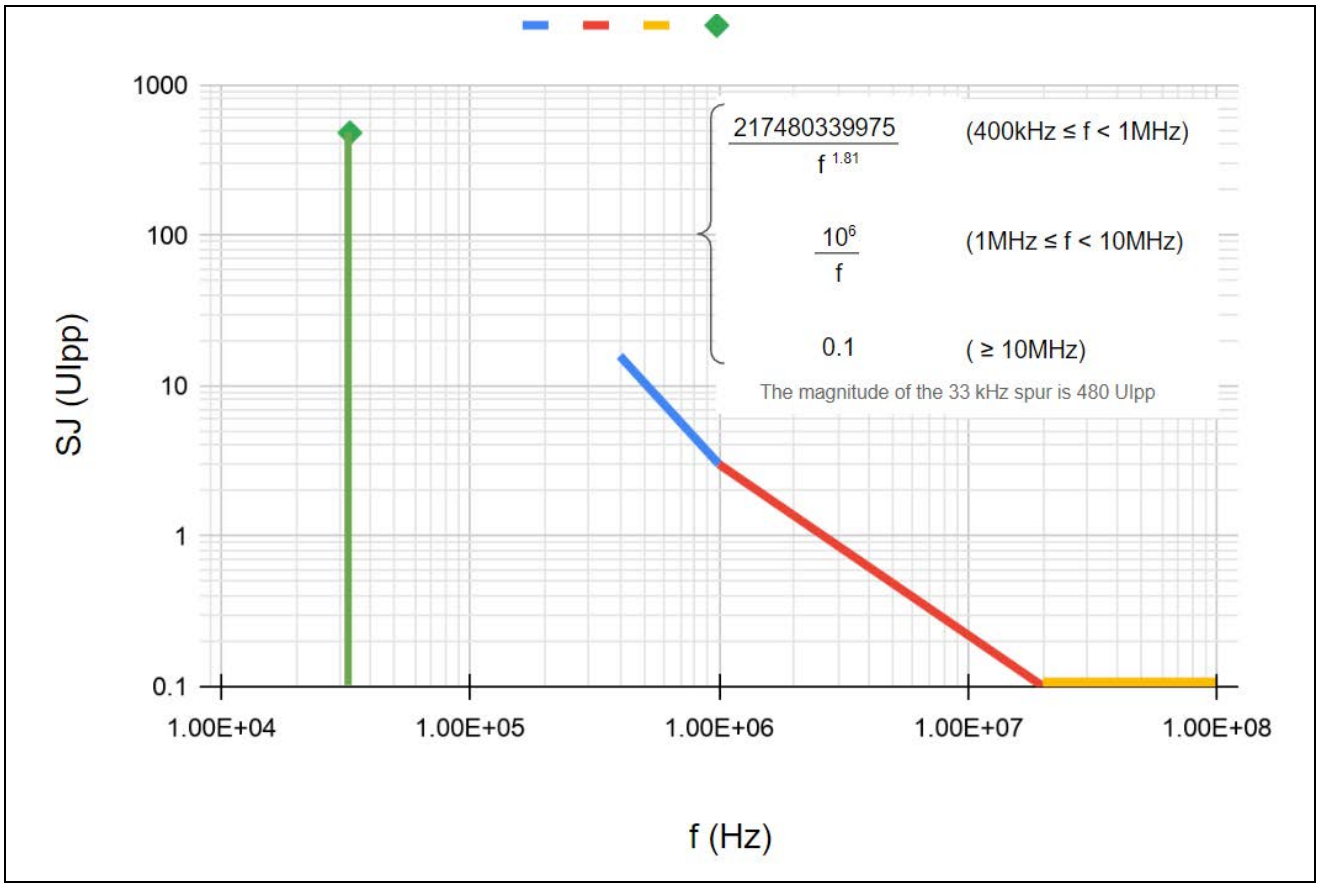
Table 5-12. Stressed jitter eye parameters

Symbol	Parameter	32.0 Gbps	OpenCAPI	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	720 - 800	720 - 800	mV_{PP}	See note 1.
T_{RX-UI}	Unit interval	31.25	31.25 (nominal)	ps	
T_{RX-ST}	Eye width	>=0.30	>=0.30	UI	See notes 2, 6.
V_{RX-ST}	Eye height	>=15	>=30	mV_{PP}	See notes 2, 6.
$T_{RX-ST-SJ}$	Swept S_J	See Figure 5-4. Sj Mask for Receivers Operating in Common Clock mode at 32.0 Gbps	See Figure 5-4. Sj Mask for Receivers Operating in Common Clock mode at 32.0 Gbps	ps	See note 3.
$T_{RX-ST-RJ}$	Random jitter	0.5	0.5	ps RMS	See note 4, 5.
$V_{RX-DIFF-INT}$	Differential noise	10	10	mV_{PP}	See notes 5, 7.
$V_{RX-CM-INT}$	Common-mode noise	150	150	mV_{PP}	See note 6.

Notes:

1. $V_{RX-LAUNCH}$ is adjusted from 720 – 800 mV for 32.0 Gbps calibration.
2. V_{RX-ST} and T_{RX-ST} are referenced to TP2P for 32.0 Gbps. Behavioral equalization is applied to the data at TP2 for 32.0 Gbps.
3. $T_{RX-ST-SJ}$ may be measured at either TP1 or TP2; 32.0 Gbps receivers are tested with an Sj mask.
4. $T_{RX-ST-RJ}$ may be adjusted to meet the target value for T_{RX-ST} at 32.0 Gbps. RJ is measured at TP1 to prevent data channel interaction from adversely affecting the accuracy of the RJ calibration. RJ is applied over the following range: the low-frequency limit may be between 1.5 - 10 MHz, and the upper limit is 1.0 GHz.
5. Both $T_{RX-ST-RJ}$ and $V_{RX-DIFF-INT}$ are limited to prevent the stressed eye from containing excessive amounts of jitter or noise distortion that are unrepresentative of a real channel. Too many of these distortion components produces a signal that cannot be equalized by an actual receiver.
6. Defined as a single tone at 120 MHz. Measurement made at TP2 without post-processing. Common mode is turned off during T_{RX-ST} and V_{RX-ST} calibration and then turned on for the stressed eye jitter test.
7. Frequency for $V_{RX-DIFF-INT}$ is chosen to be slightly above the first pole of the reference CTLE.
8. Applied for Common Clock testing only as a triangular phase modulation with a frequency between 30 kHz - 33 kHz when testing at 32.0 Gbps.

Figure 5-4. Sj Mask for Receivers Operating in Common Clock mode at 32.0 Gbps



5.6.4 Differential return loss for both transmitter and receiver

The differential return loss curve from the OIF CEI-28G-MR Specification is shown in *Figure 5-5*. Parameters SDD11 and SDD22 are the OIF CEI-28G-MR compliance curve.

Table 5-13. Receiver differential return loss parameters (from OIF CEI-28G-MR Specification)

Parameter	Value	Units
A0	-12	dB
f0	0	MHz
f1	0.1714 × R_Baud	Hz
f2	R_Baud	Hz
Slope	12.0	dB/dec

Figure 5-5. SDD11 and SDD22 differential return loss at c4 (pads) template for RX and TX (from OIF CEI-28G-MR Specification)

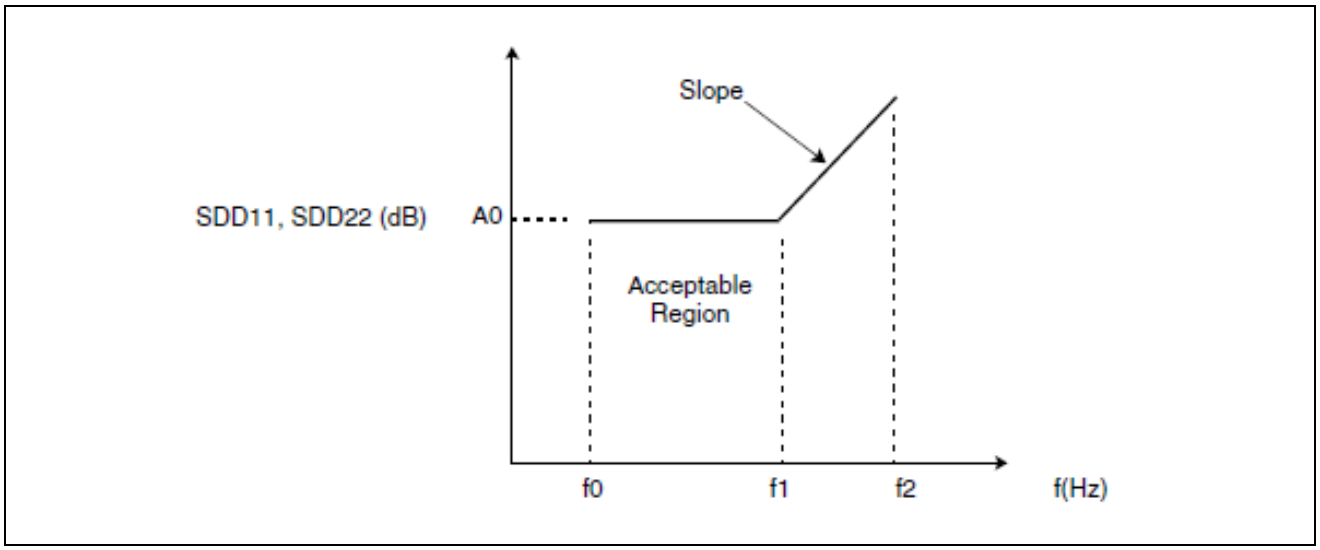
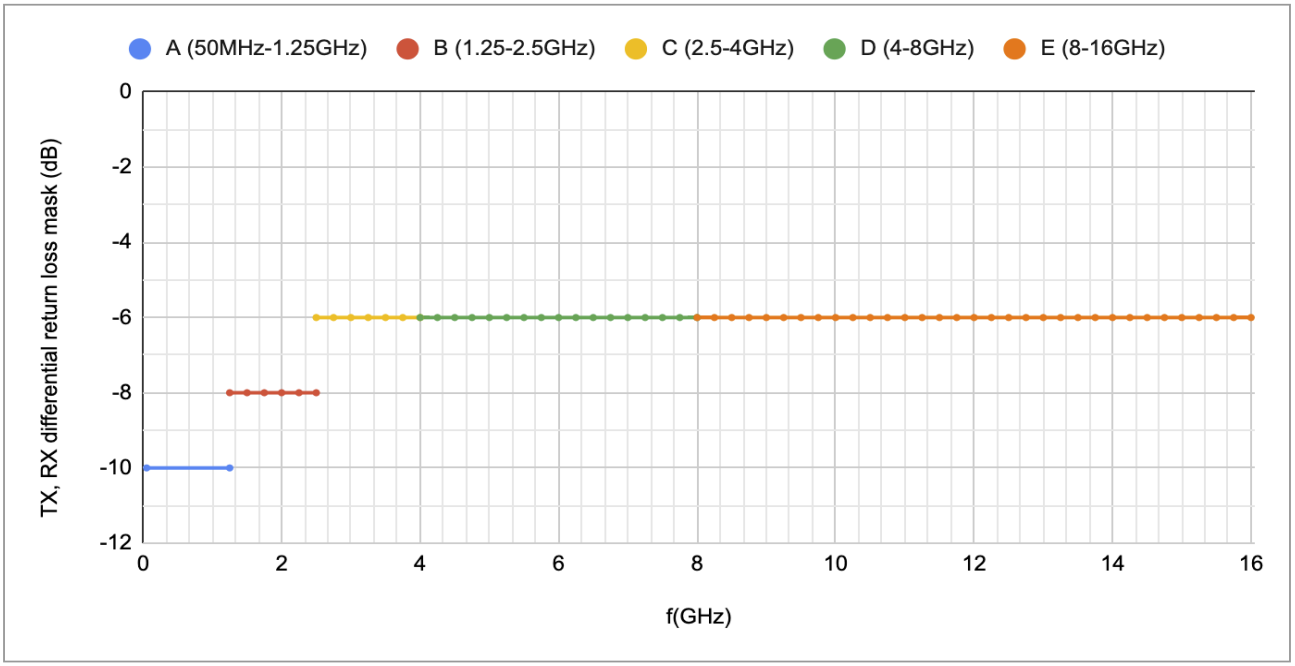


Figure 5-6. TX, RX differential return loss mask with 42.5 Ω reference



Note 1 (for Figure 5-6): If you are using 50 Ω reference and the VNA does not offer port reference impedance transformation from 50 Ω to 42.5 Ω you should expect up to a ~2 dB penalty on the return loss in the low frequency region.

Note 2: For inter-operability for PCIe and OIF, a device must meet the return loss specifications outlined in Figures 5-5 and 5-6.

5.6.5 Common-to-differential mode and differential-to-common mode conversion

The common-to-differential mode and differential-to-common mode conversion specifications are intended to limit the amount of unwanted signal energy that is allowed to be generated due to conversion of common-mode voltage to differential-mode voltage or vice-versa. When measured at the respective input test point, common-to-differential mode or differential-to-common mode conversion must not exceed the limits illustrated in *Figure 5-7. SDC11 and SCD11 for module input (TP1) and host input (TP4a) (for fb = 32 GHz).*

Note: *Figure 5-7. SDC11 and SCD11 for module input (TP1) and host input (TP4a) (for fb = 32 GHz)* is the OIF CEI-28G-MR compliance curve given by Equation Y.

Equation Y:

SDC11, SCD11 < -22 + 14 × (f/fb) dB for 0.05 < f < fb/2
SDC11, SCD11 < -18 + 6 × (f/fb) dB for fb/2 < f < fb

Figure 5-7. SDC11 and SCD11 for module input (TP1) and host input (TP4a) (for fb = 32 GHz)

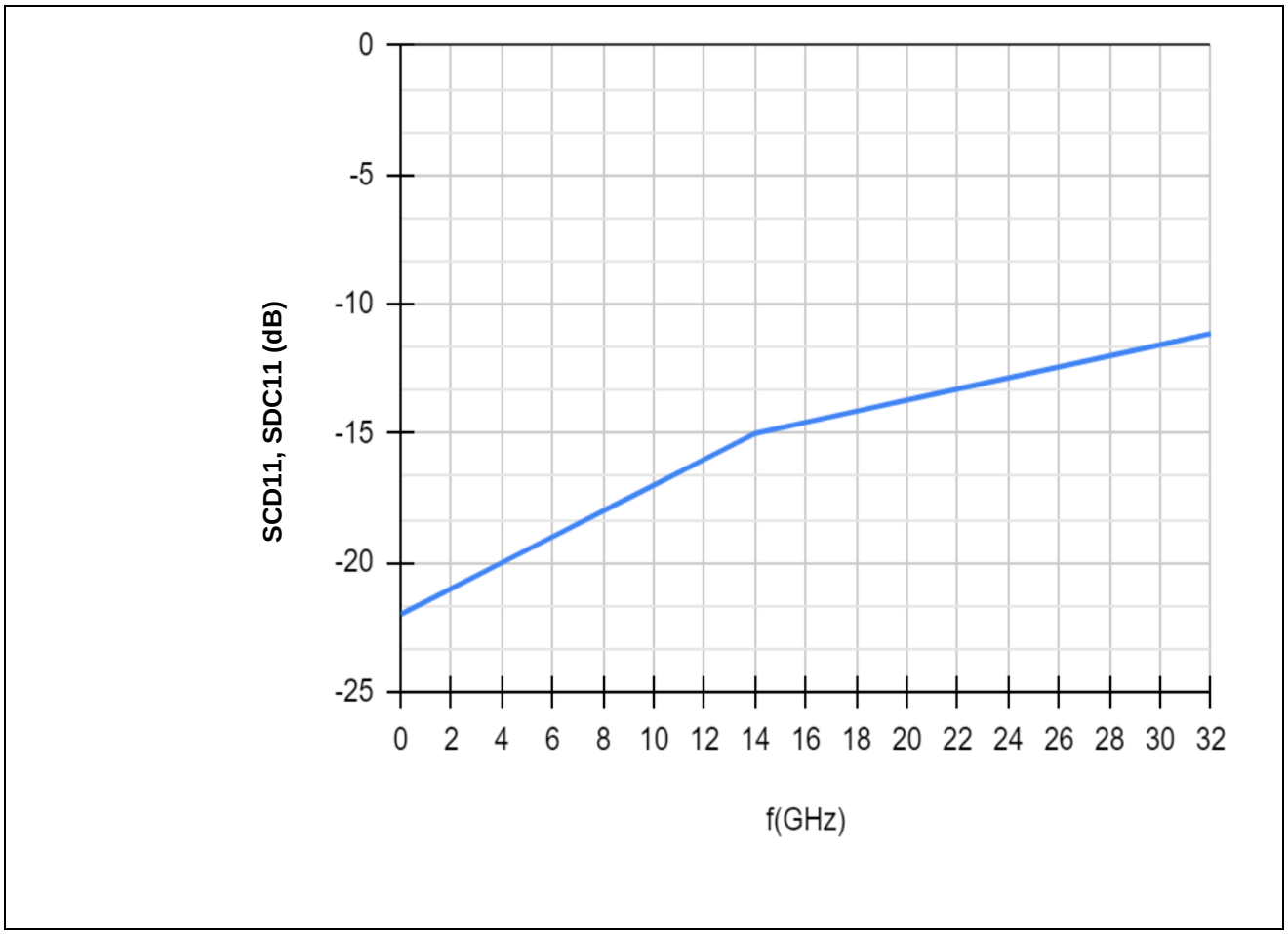
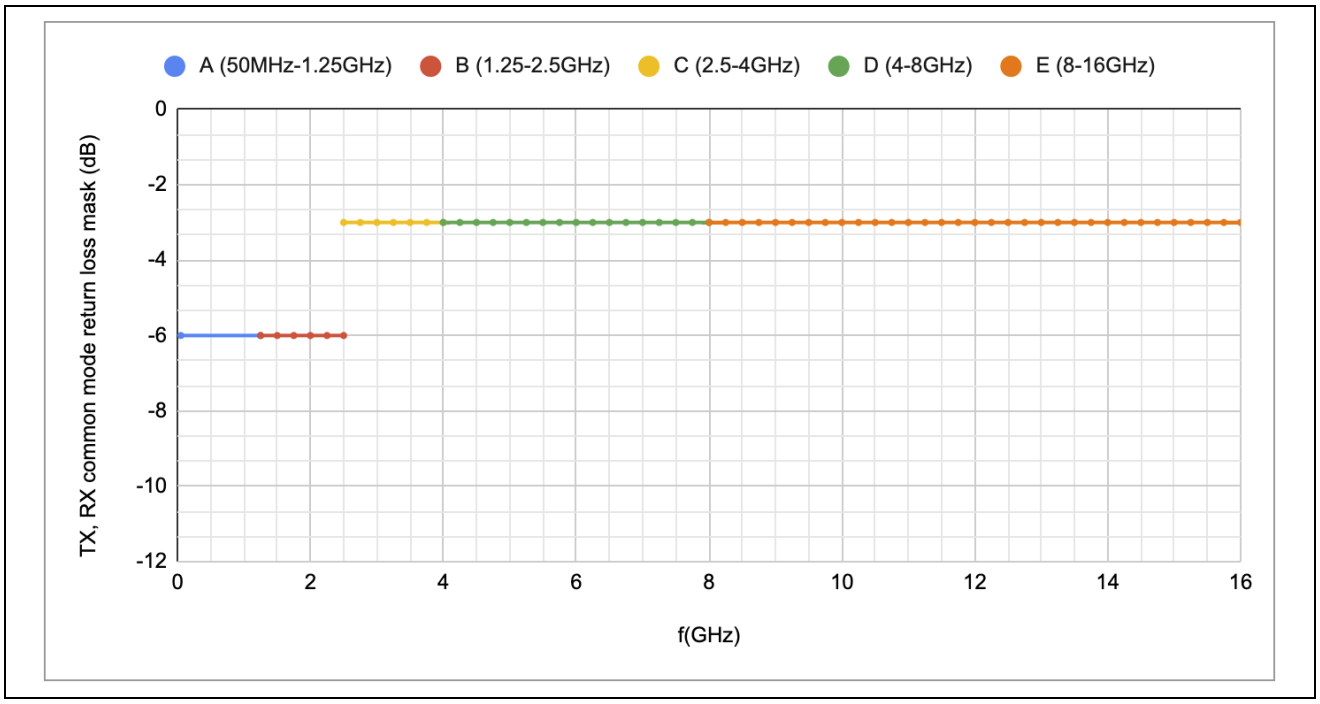


Figure 5-8. TX, RX common mode return loss mask with 42.5 Ω reference



Note (for Figure 5-8): If you are using a 50 Ω reference and the VNA does not offer port reference impedance transformation from 50 Ω to 42.5 Ω, you should expect up to a ~1 dB penalty on the return loss in the low-frequency region.

5.7 Characterizing channel common mode noise

A channel must meet the common-mode requirements as they are defined in the receiver specification. In general, it is not possible to accurately simulate all the channel's common-mode noise contributions due to the large number of mechanisms that can generate CM noise, including the transmitter. Typically, channel common-mode noise is a budgeted parameter, and the limits defined below assume a budgeting process. The channel's CM limit is defined as the amount of CM noise that a channel can add and still meet the RX CM limits assuming the worst-case TX CM. This limit is 75 mV_{PP} for EH < 100 mV and 125 mV_{PP} for EH ≥ 100 mV_{PP}.

Note that the TX and channel CM noise parameters cannot simply be added to obtain the RX CM limit. This is due to the fact that a channel will attenuate some of the high-frequency TX CM noise while propagating TX LF CM noise through with little loss. The channel may also contribute both high- and low-frequency CM components of its own.

6. Compliance

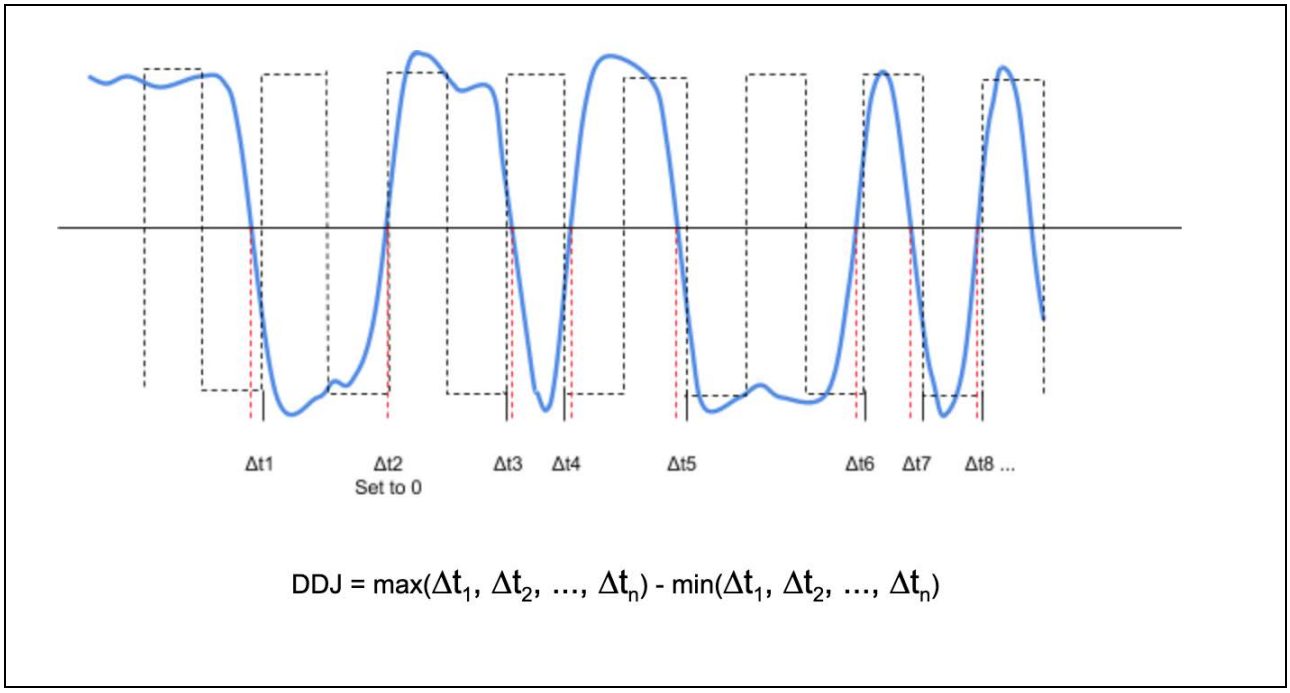
6.1 Overview

Channel designs interfacing with an OpenCAPI 32 Gbps compliant processor are expected to deviate somewhat from the *OIF CEI-28G-MR* specification. However, it is likely that the endpoint PHY is MR compliant. The endpoint PHY most likely has more RX equalization than would be optimal; however, it should be adequate.

6.2 Data dependent jitter (DDJ) measurement

Using a high-resolution oscilloscope analyzer, establish a crossing level equal to the average value of the entire waveform being measured. *Figure 6-1* illustrates this method. The vertical axis is in arbitrary units and the horizontal axis is plotted in UI. The AC waveform is coupled to an average value of zero. Therefore, zero is the appropriate crossing level. The rectangular waveform shows the expected crossing times. The other plot is the waveform with jitter that is being measured. Only 16 UI are shown in this example. The waveforms have been arbitrarily aligned with (delta_t2 = 0) at 4 UI.

Figure 6-1. DDJ measurement method



6.3 Endpoint-compliance TX jitter models for channel simulation

A TX model for compliance will be formulated as follows:

- The jitter terms are specified at the PAD or c4 of the chip.
- The carrier organic package is considered part of the channel.

Using the dual Dirac jitter model1, total jitter (TJ) is given by equation (1); where Q(BER) is Q-factor, both RJ and BUJ are assumed as Gaussian terms down to 1e-15 probability; σ_{RJ} and σ_{BUJ} are RMS values for RJ and BUJ respectively. Equation (1) can be rewritten in terms of peak-to-peak values of RJ and BUJ as shown in equation (2). *Figure 6-2* illustrates equation (1) and equation (2).

Figure 6-2. Jitter model equations

Total jitter is defined as shown in Equation (1).

Equation (1):

$$T_{TJ} = T_{DCD} + T_{DDJ} + 2Q\,(BER)\sqrt{\sigma_{RJ}^2 + \sigma_{BUJ}^2}$$

Total jitter in terms of peak-to-peak values of RJ and BUJ is defined as shown in Equation (2).

Equation (2):

$$T_{TJ} = T_{DCD} + T_{DDJ} + \sqrt{T_{RJ}^2 + T_{BUJ}^2}$$

For equation (1) and equation (2): T_{DDJ} = 0.0329 UI, T_{DCD} = 0.035 UI, T_{RJ} = 0.15 UI, T_{BUJ} = 0.15 UI, T_{TJ} = 0.28 UI

Note: Specifying the upper bounds for T_{DCD}, T_{RJ}, T_{BUJ}, T_{TJ}, implicitly specifies the upper limit for T_{DDJ}.

6.4 Receiver compliance

See the receiver compliance section of the *OIF CEI-28G-MR Specification* for additional details.

Appendix A IBM POWER10-specific information

This section describes IBM POWER10-specific details.

A.1 Global parameters

Table A-1. Global parameters

Parameter	Specification			
Data rate	32.0 Gbps for JEDEC Applications; 31.875 Gbps for over-clocked OIF Applications.			
POWER10 I/O power supply	Process	Minimum	Typical	Maximum
	V_{IO}	0.8 V	0.9 V	0.95 V
	Note: V_{DN} (logic supply) = 0.72 V nominal and is adaptive.			
POWER10 junction temperature (T_J)	-10°C to 85°C			
Termination	85 Ω differential at RX, POWER10 TX is SST with 42.5 Ω from V_{IO}-to-PAD and 42.5 Ω from PAD-to-GND (85 Ω is a deviation from the *OIF CEI-28G-MR Specification*, which defines the nominal impedance as 100 Ω).			
ESD	1000 V HBM, 200 V CDM. (This is outside of the *OIF CEI-28G-MR Specification.*)			
POWER10 link latency	PHY-to-TX driver output; 17 UI. RX-sampler-to-PHY interface: 17 UI.			

A.2 POWER10 nominal estimated power dissipation

The power budget breakdown at 32 Gbps for some of the shared blocks outside of the I/O lane, such as the PLL, are amortized per-lane values. The overall link efficiency is targeted around 5 - 6 pJ/b at 32 Gbps (1TX + 1RX + PLL). The PLL is amortized over 16 lanes in the POWER10 processor.

A.3 Channel definition

A.3.1. Electrical specification for POWER10 TX

Table A-2. Electrical specification for POWER10 TX

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
F_b	Baud rate		32.0 Gbps for JEDEC applications 31.875 Gbps for over-clocked OIF applications		Gbps	
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage	800	1100	1300	mV	TX launch into a DC matched 85 Ω system.
$V_{TX\text{-}CM\text{-}DC}$	TX output CM	0.475	0.5	0.562	V	CM during normal operation and during RxCAL mode for DC coupled systems.
$V_{TX\text{-}CM\text{-}AC}$	AC CM ripple			25	mVp	Measured up to F_{BAUD}.
V_{DIFF_RxCAL}		-10	0	10	mV	Differential voltage during RxCAL.
RTX_{RxCAL}	Impedance during RxCAL	95		170	Ω	
TR_{TX}	Rise/fall time at TX			6.875	ps	20% - 80%, in TX S-parameters
TX_S21	Insertion loss at Nyquist	-0.5			dB	POWER10 TX has boot, from simulation
TX FIR	TX De-emphasis:					$\|C_0\| + \|C_{+1}\| + \|C_{-1}\| = 1$
	C-1					C_i resolution to be better than 1/36.
	C0					
	C+1					POWER10 does not implement (C+1)

A.3.2. POWER10 TX jitter terms

The jitter terms are specified at the pad or c4 on the chip. The carrier organic package is considered part of the channel. For POWER10 jitter terms for simulations or TX silicon, the S-parameters models are available upon request to the OpenCAPI PHY Signaling Workgroup chair.

A.3.3. POWER10 TX SST termination excluding T-coils and ESD

Figure A-1. POWER10 TX SST termination excluding T-coils and ESD